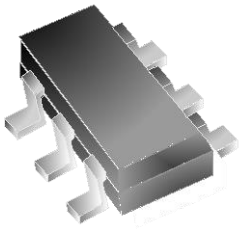
DW05-4R-S

Features

- Solid-state silicon-avalanche technology
- 350 Watts Peak Pulse Power per Line (t_p=8/20μs)
- Low operating and clamping voltage
- Up to four I/O Lines of Protection
- Low Leakage
- Low operating voltage:5V



SOT-23-6L

IEC Compatibility (EN61000-4)

- IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 15A (8/20μs)

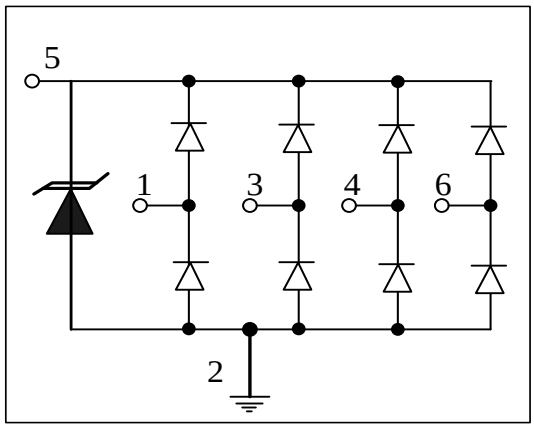
Mechanical Characteristics

- SOT-23-6L package
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS Compliant

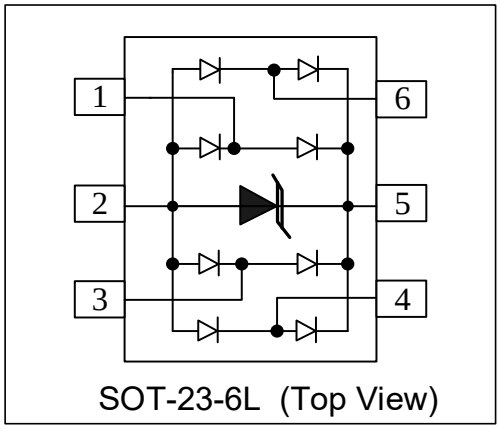
Applications

- Video/Graphics Card
- Handheld & Portable Electronics
- PC/Notebook USB2.0/IEEE1394 ports
- 10/100/1000 Ethernet
- DVI interfaces
- Wireless data (WAN/LAN) systems

Circuit Diagram



Schematic & PIN Configuration

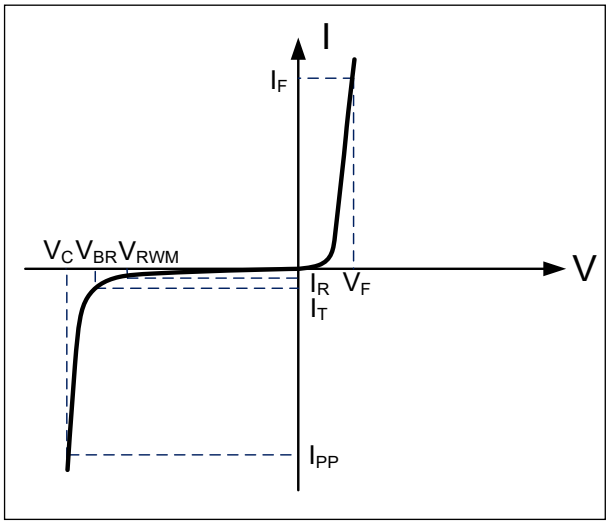


SOT-23-6L (Top View)

Absolute Maximum Rating			
Rating	**Symbol**	**Value**	**Units**
Peak Pulse Power (t_p =8/20μs)	P_{PP}	350	Watts
Peak Pulse Current (t_p =8/20μs)	I_{pp}	15	A
Operating Temperature	T_J	-55 to + 125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Parameters (T=25℃)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical Characteristics

DW05-4R-S						
Parameter	**Symbol**	**Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	6.0			V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25℃			0.5	μA
Forward Voltage	V_F	I_T=1mA			1.5	V
Clamping Voltage	V_C	I_{PP}=15A, t_p=8/20μs Any I/O pin to GND		20	23	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz I/O pin to GND		1.5	2.0	pF
		V_R = 0V, f = 1MHz Between I/O pins		0.75	1.0	pF

Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

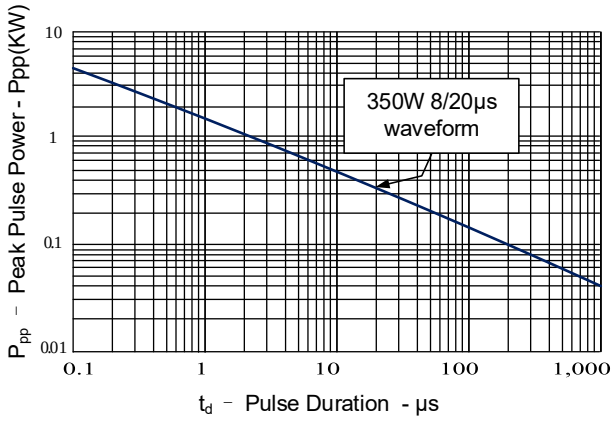


Figure 2: Power Derating Curve

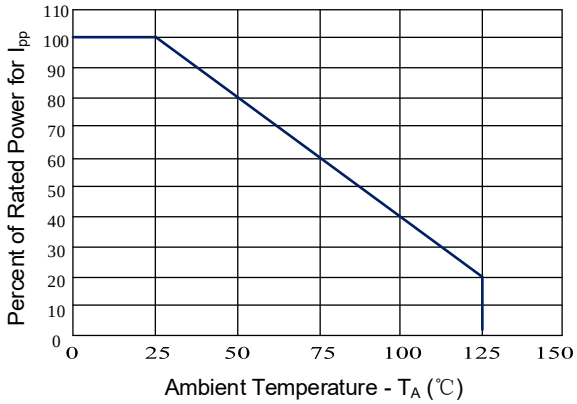


Figure 3: Pulse Waveform

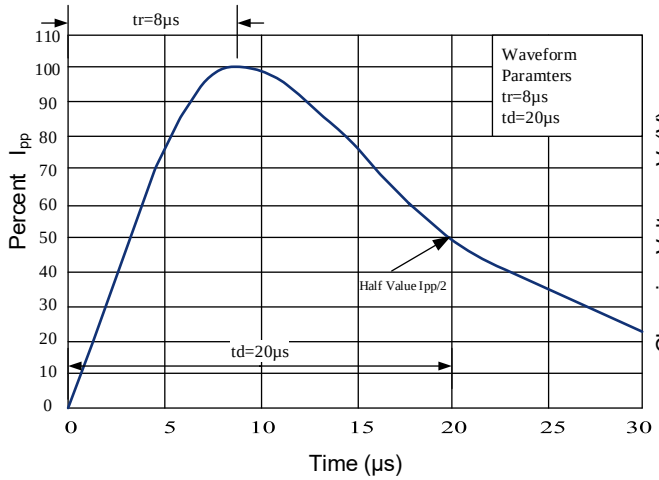


Figure 4: Clamping Voltage vs. Peak Pulse Current

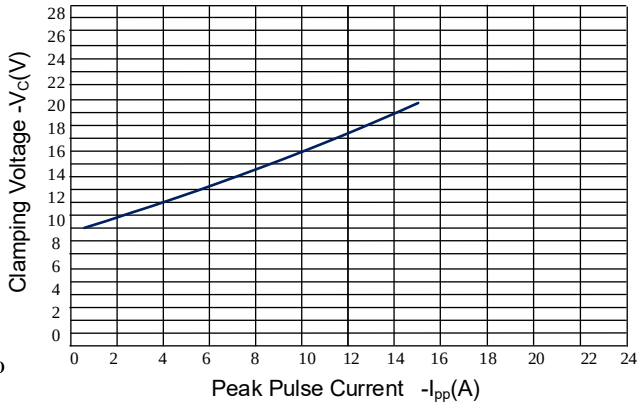


Figure 5: Capacitance vs. Reverse Voltage

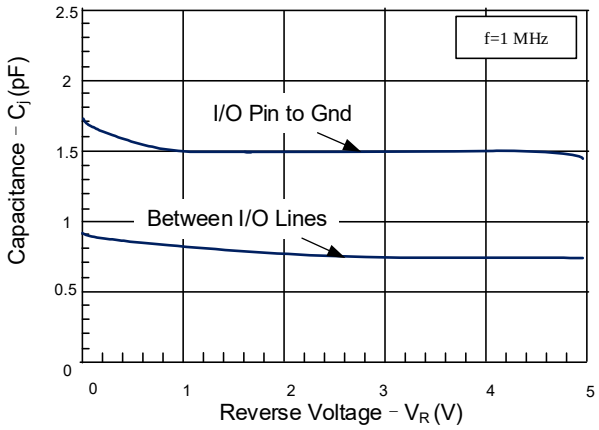
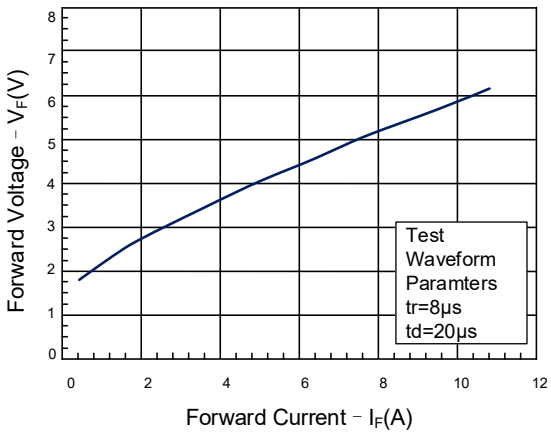


Figure 6: Forward Voltage vs. Forward Current



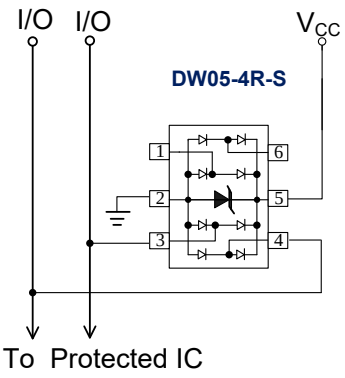
Application Information

Device Connection Options for Protection of Four High-Speed Data Lines

The DW05-4R-S TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (R_{EF1}) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (R_{EF2}) is connected at pin 5. The options for connecting the positive reference are as follows:

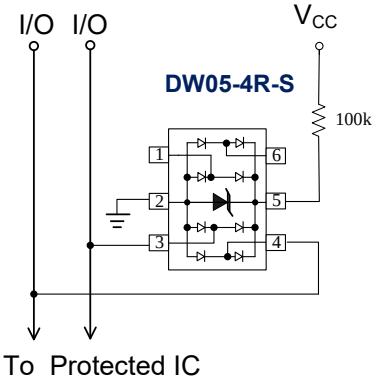
1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail (V_{cc}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over- voltage to the supply rail.

Data Line and Power Supply Protection Using V_{CC} as reference



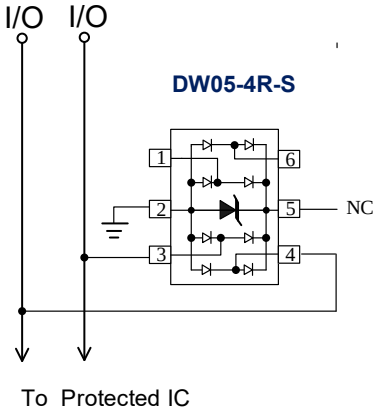
2. The DW05-4R-S can be isolated from the power supply by adding a series resistor between pin 4 and V_{CC}. A value of 100kΩ is recommended. The internal TVS and steering diodes remains biased, providing the advantage of lower capacitance.

Data Line Protection with Bias and Power Supply Isolation Resistor



3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

Data Line Protection Using Internal TVS Diode as Reference



Typical Applications

Video Interface Protection

Video interfaces are susceptible to transient voltages resulting from electrostatic discharge (ESD) and "hot plugging" cables. If left unprotected, the video interface IC may be damaged or even destroyed. Protecting a high-speed video port presents some unique challenges. First, any added protection device must have extremely low capacitance and low leakage current so that the integrity of the video signal is not compromised. Second, the protection component must be able to absorb high voltage transients without damage or degradation. As a minimum, the device should be rated to handle ESD voltages per IEC 61000-4-2, level 4 (±15kV air, ±8kV contact). The clamping voltage of the device (when conducting high current ESD pulses) must be sufficiently low enough to protect the sensitive CMOS IC. If the clamping voltage is too high, the "protected" device may latch-up or be destroyed. Finally, the device must take up a relatively small amount of board space, particularly in portable applications such as notebooks and handhelds. The DW05-4R-S is designed to meet or exceed all of the above criteria. A typical video interface protection circuit is shown in Figure 1. All exposed lines are protected including R, G, B, H-Sync, V-Sync, and the ID lines for plug and play monitors.

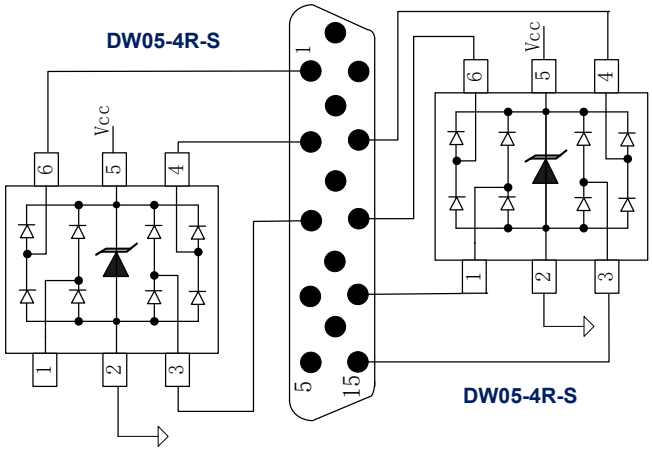


Figure 1 Video Interface Protection

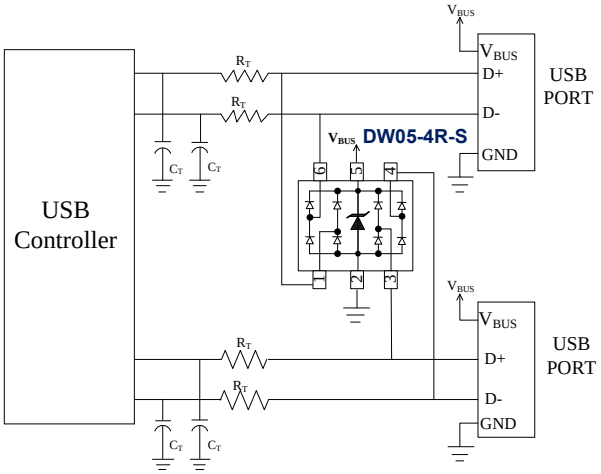


Figure 2 Dual USB Port Protection

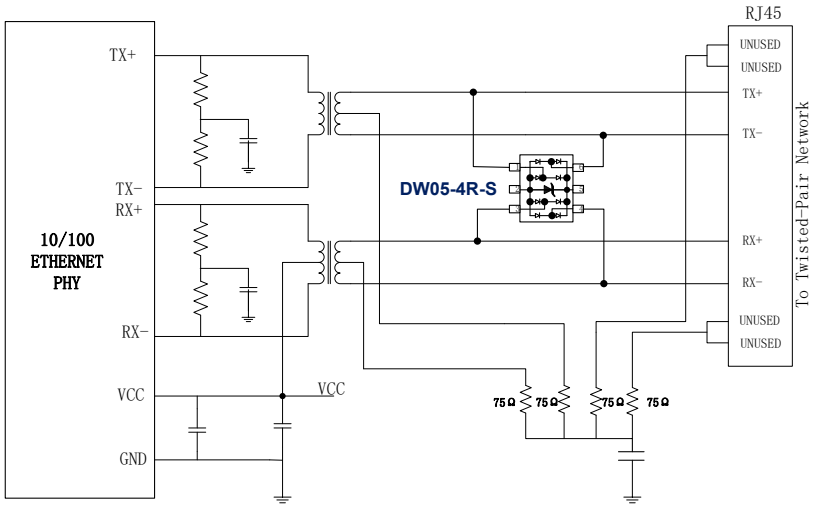
Universal Serial Bus ESD Protection

The DW05-4R-S may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure 2). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

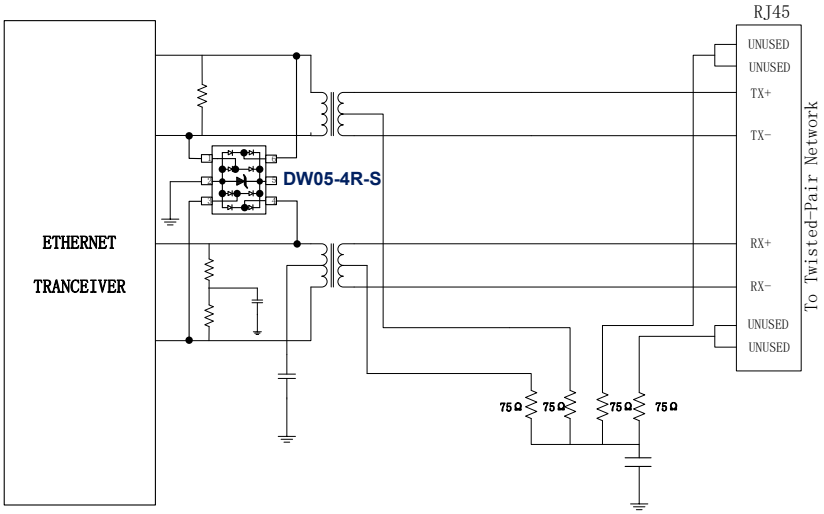
10/100 ETHERNET PROTECTION

Ethernet ICs are vulnerable to damage from electrostatic discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC 61000-4-2. If the discharge is catastrophic, it will destroy the protected IC. If it is less severe, it will cause latent failures that are very difficult to find.

10/100 Ethernet operates at 125MHz clock over a twisted pair interface. In a typical system, the twisted pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmit or receive line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 3 shows how to design the DW05-4R-S on the line side of a 10/100 Ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. If more common mode protection is needed, figure 4 shows how to design the DW05-4R-S on the IC side of the 10/100 Ethernet circuit to provide differential and common mode protection. The DW05-4R-S cannot be grounded on the line side because the hi-pot test requires the line side not to be grounded.



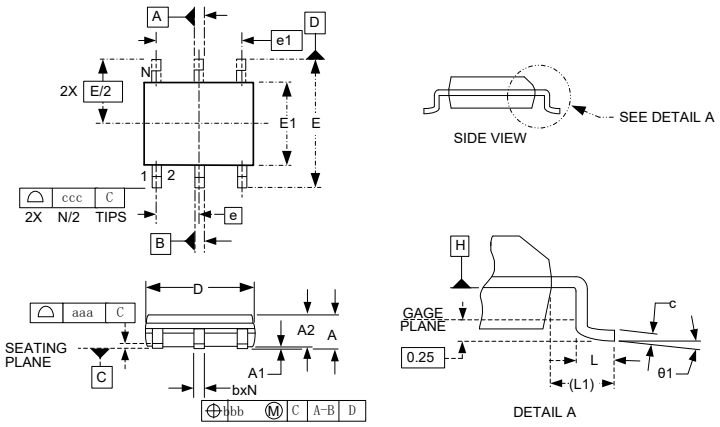
10/100 Ethernet Differential Protection



10/100 Ethernet Differential and Common Mode Protection

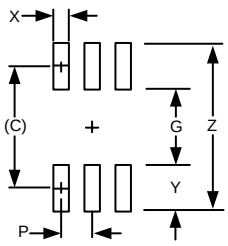
Outline Drawing – SOT-23-6L

PACKAGE OUTLINE



NOTES:

1. Controlling Dimensions are In Millimeters (Angles In Degrees).
2. Datums -A- And -B- To Be Determined At Datum Plane -H-.
3. Dimensions “E1” And “D” Do Not Include Mold Flash，Protrusions Or Gate Burrs.



SOT-23-6L

DIMENSIONS

DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	0.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.122	2.80	2.90	3.10
E1	.060	.063	.069	1.50	1.60	1.75
E	.110BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
θ1	0°	-	10°	0°	-	10°
N	6			6		
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

Notes

THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Codes

Part Number	DW05-4R-S
Marking Code	5UB

Package Information

Qty：3k/Reel